What is claimed is:

1. A method of creating interconnect metal, comprising the steps of:

providing a substrate, at least one point of electrical contact having been provided over the surface of said substrate;

depositing a first layer of semiconductor material over the surface of said substrate, including the surface of said at least one point of electrical contact having been provided over the surface of said substrate;

patterning and etching said first layer of semiconductor material, creating at least one first opening through said first layer of semiconductor material that aligns with said at least one point of electrical contact having been provided over the surface of said substrate;

creating at least one first conductive via in said at least one first opening created through said first layer of semiconductor material;

depositing a first layer of conductive material over the surface of said first layer of semiconductor material, including the surface of said at least one first conductive via created in said at least one first opening created through said first layer of semiconductor material; and

patterning and etching said first layer of conductive material, creating at least one first wide-line of interconnect metal over the surface of said first layer of semiconductor material overlying said

at least one first conductive via created in said at least one first opening created through said first layer of semiconductor material, said at least one first conductive via and said at least one first wide-line of interconnect metal making contact in a first interface area, additionally creating at least one first slot through said first layer of conductive material being separated from said first interface area by a measurable distance.

2. The method of claim 1, said at least one first slot being separated from said first interface area by a measurable distance comprising:

a first, a second and a third surface area or a combination thereof;

said first surface area being a rectangle or a square;

said second surface area being a rectangle or a square;

said third surface area being a rectangle or a square;

a side of said first surface area being parallel with a first side of said at least one first conductive via;

a side of said second surface area being parallel with a second side of said at least one first conductive via;

a side of said third surface area being parallel with a third side of said at least one first conductive via;

a side of said first surface area being separated from a first side of said at least one first conductive via by a measurable distance;

a side of said second surface area being separated from a second side of said at least one first conductive via by a measurable distance; and

a side of said third surface area being separated from a third side of said at least one first conductive via by a measurable distance.

3. The method of claim 2, said first surface area having dimensions of about 0.24 x 0.8 μm^2.

4. The method of claim 2, said second surface area having dimensions of about 0.24 x 0.8 μm^2.

5. The method of claim 2, said third surface area having dimensions of about 0.24 x 1.19 μm^2.

6. The method of claim 2, said first surface area being separated in an X-direction from a first side of said at least one first via by a distance of about 0.2 μm.

7. The method of claim 2, said second surface area being separated in an X-direction from a second side of said at least one first via by a distance of about 0.2 μm.

8. The method of claim 2, said third surface area being separated in an Y-direction from a third side of said at least one first via by a distance of about 0.15 μm.

9. The method of claim 1, said first layer of semiconductor material comprising a dielectric material.

10. The method of claim 1, said at least one first conductive via created in said at least one opening through said first layer of semiconductor material comprising copper.

11. The method of claim 1, said first layer of conductive material deposited over the surface of said first layer of semiconductor material comprising copper.

12. The method of claim 1, said first wide-line of interconnect metal overlying said at least one first conductive via having a width of about at least 2 μm.

13. The method of claim 1, additionally comprising the steps of:

depositing a second layer of semiconductor material over the surface of said first layer of semiconductor material, including the surface of said at least one first wide-line of interconnect metal

created over the surface of said first layer of semiconductor material;

patterning and etching said second layer of semiconductor material, creating at least one second opening through said second layer of semiconductor material that aligns with said at least one first wide-line of interconnect metal created over the surface of said first layer of semiconductor material;

creating at least one second conductive via in said at least one second opening created through said second layer of semiconductor material;

depositing a second layer of conductive material over the surface of said second layer of semiconductor material, including the surface of said at least one second conductive via created in said at least one second opening created through said second layer of semiconductor material; and

patterning and etching said second layer of conductive material, creating at least one second wide-line of interconnect metal over the surface of said second layer of semiconductor material overlying said at least one second conductive via created in said at least one second opening created through said second layer of semiconductor material, said at least one second conductive via and said at least one second wide-line of interconnect metal making contact in a second interface area, additionally creating at least one second slot through said

second layer of conductive material being separated from said second interface area by a measurable distance.

14. The method of claim 13, said at least one second slot being separated from said second interface area by a measurable distance comprising:

a first, a second and a third surface area or a combination thereof;

said first surface area being a rectangle or a square;

said second surface area being a rectangle or a square;

said third surface area being a rectangle or a square;

a side of said first surface area being parallel with a first side of said at least one second conductive via;

a side of said second surface area being parallel with a second side of said at least one second conductive via;

a side of said third surface area being parallel with a third side of said at least one second conductive via;

a side of said first surface area being separated from a first side of said at least one second conductive via by a measurable distance;

a side of said second surface area being separated from a second side of said at least one second conductive via by a measurable distance; and

a side of said third surface area being separated from a third side of said at least one second conductive via by a measurable distance.

15. The method of claim 14, said first surface area having dimensions of about 0.24 x 0.8 μm^2.

16. The method of claim 14, said second surface area having dimensions of about 0.24 x 0.8 μm^2.

17. The method of claim 14, said third surface area having dimensions of about 0.24 x 1.19 μm^2.

18. The method of claim 14, said first surface area being separated in an X-direction from a first side of said at least one second via by a distance of about 0.2 μm.

19. The method of claim 14, said second surface area being separated in an X-direction from a second side of said at least one second via by a distance of about 0.2 μm.

20. The method of claim 14, said third surface area being separated in an Y-direction from a third side of said at least one second via by a distance of about 0.15 μm.

21. The method of claim 13, said second layer of semiconductor material comprising a dielectric material.

22. The method of claim 13, said at least one second conductive via created in said at least one opening through said second layer of semiconductor material comprising copper.

23. The method of claim 13, said second layer of conductive material deposited over the surface of said first layer of semiconductor material comprising copper.

24. The method of claim 13, said second wide-line of interconnect metal overlying said at least one second conductive via having a width of about at least 2 μm.

25. A method of creating interconnect metal, comprising the steps of:

providing a substrate, at least one point of electrical contact having been provided over the surface of said substrate;

creating at least one layer of interconnect metal over the surface of said substrate, said at least one layer of interconnect metal comprising at least one interconnect via in addition to comprising at least one layer of wide-line interconnect metal, said at least one interconnect via overlying said at least one point of

electrical contact having been provided over the surface of said substrate, said at least wide-line of interconnect metal overlying said at least one interconnect via, said at least one interconnect via and said at least one wide-line interconnect metal making contact in a interface area, additionally creating at least one slot through said at least one wide-line interconnect metal being separated from said interface area by a measurable distance.

26. The method of claim 25, said creating at least one layer of interconnect metal over the surface of said substrate comprising the steps of:

depositing a layer of semiconductor material over the surface of said substrate, including the surface of said at least one point of electrical contact provided over the surface of said substrate;

patterning and etching said layer of semiconductor material, creating at least one opening through said layer of semiconductor material that aligns with said at least one point of electrical contact provided over the surface of said substrate;

creating at least one conductive via in said at least one opening created through said layer of semiconductor material;

depositing a layer of conductive material over the surface of said layer of semiconductor material, including the surface of said at least one conductive via created in said at least one opening created through said layer of semiconductor material; and

patterning and etching said layer of conductive material, creating at least one wide-line of interconnect metal over the surface of said layer of semiconductor material overlying said at least one conductive via created in said at least one opening created through said layer of semiconductor material, said at least one conductive via and said at least one wide-line of interconnect metal making contact in an interface area, additionally creating at least one slot through said layer of conductive material being separated from said interface area by a measurable distance.

27. The method of claim 26, said at least one slot being separated from said interface area by a measurable distance comprising:

a first, a second and a third surface area or a combination thereof;

said first surface area being a rectangle or a square;

said second surface area being a rectangle or a square;

said third surface area being a rectangle or a square;

a side of said first surface area being parallel with a first side of said at least one conductive via;

a side of said second surface area being parallel with a second side of said at least one conductive via;

a side of said third surface area being parallel with a third side of said at least one conductive via;

a side of said first surface area being separated from a first side of said at least one conductive via by a measurable distance;

a side of said second surface area being separated from a second side of said at least one conductive via by a measurable distance; and

a side of said third surface area being separated from a third side of said at least one conductive via by a measurable distance.

28. The method of claim 27, said first surface area having dimensions of about 0.24 x 0.8 μm^2.

29. The method of claim 27, said second surface area having dimensions of about 0.24 x 0.8 μm^2.

30. The method of claim 27, said third surface area having dimensions of about 0.24 x 1.19 μm^2.

31. The method of claim 27, said first surface area being separated in an X-direction from a first side of said at least one second via by a distance of about 0.2 μm.

32. The method of claim 27, said second surface area being separated in an X-direction from a second side of said at least one second via by a distance of about 0.2 μm.

33. The method of claim 27, said third surface area being separated in an Y-direction from a third side of said at least one second via by a distance of about 0.15 μm.

34. The method of claim 26, said layer of semiconductor material comprising a dielectric material.

35. The method of claim 26, said at least one conductive via created in said at least one opening through said layer of semiconductor material comprising copper.

36. The method of claim 26, said layer of conductive material deposited over the surface of said substrate comprising copper.

37. The method of claim 26, said wide-line of interconnect metal overlying said at least one conductive via having a width of about at least 2 μm.

38. The method of claim 2, a side of said first surface area overlying a side of said third surface area over a measurable distance.

39. The method of claim 2, a side of said second surface area overlying a side of said third surface area over a measurable distance.

40. The method of claim 2, a side of said first surface area and a side of said second surface area overlying a side of said third surface area over a measurable distance.

41. The method of claim 14, a side of said first surface area overlying a side of said third surface area over a measurable distance.

42. The method of claim 14, a side of said second surface area overlying a side of said third surface area over a measurable distance.

43. The method of claim 14, a side of said first surface area and a side of said second surface area overlying a side of said third surface area over a measurable distance.

44. The method of claim 27, a side of said first surface area overlying a side of said third surface area over a measurable distance.

45. The method of claim 27, a side of said second surface area overlying a side of said third surface area over a measurable distance.

46. The method of claim 27, a side of said first surface area and a side of said second surface area overlying a side of said third surface area over a measurable distance.